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;PALASM Design Description

;--------------------------- Declaration Segment ---------------------

TITLE     XHATCH11 - Crosshatch Generator
PATTERN   U117 of Control Board
REVISION  1.1
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COMPANY   ELECTROHOME LTD.
DATE      12/14/92

CHIP  XHATCH  PALCE16V8

;---------------------------- Description -----------------------------
;
; This PAL, with the aid of delay line U109, creates four types of
; test patterns; standard crosshatch, dense crosshatch, dot field
; and crosshatch with dots. Horizontal crosshatch lines are created
; using ATC from PLD U111 and VLTC from the vertical RAM circuit (U102
; etc). Vertical lines are created using HX and HC3 from U111. The HX
; signal is composed of 32 narrow pulses on every scan line. Each pulse
; has a width of one half cycle of clock signal PIXCLKB from the DPB.
; HX is input to the delay line, which outputs delayed versions TAP1 to
; TAP7, each delayed by a multiple of 5 nsec. These are input to the
; PAL, which selects one of the signals according to the code 'K'
; formed by W0-W2 from register U94. The delayed pulses are ORed with
; the first tap. This narrows the width of the pulses, resulting in
; thinner vertical crosshatch lines. The width is chosen by software
; according to the horizontal scan frequency.
;
; The horizontal and vertical lines are ANDed to create a crosshatch
; and ORed to create dots. S0 (SELECT0) and S1 (SELECT1) from
; register U94 select one of the four possible test patterns for output
; on XHATCH. This output is mixed with text pixels in PAL U108.
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; Revision History:
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;   V1.0 - original
;   V1.1 - changed code K=1 to give 0 ns delay instead of 5 ns to
;          make brighter vertical lines for 80 kHz - 100 kHz
;
;--------------------------- PIN Declarations --------------------------

PIN   1  TAP1     COMBINATORIAL ; INPUT  delay line output - 5 ns
PIN   2  TAP2     COMBINATORIAL ; INPUT  delay line output - 10 ns
PIN   3  TAP3     COMBINATORIAL ; INPUT  delay line output - 15 ns
PIN   4  TAP4     COMBINATORIAL ; INPUT  delay line output - 20 ns
PIN   5  TAP5     COMBINATORIAL ; INPUT  delay line output - 25 ns
PIN   6  TAP6     COMBINATORIAL ; INPUT  delay line output - 30 ns
PIN   7  TAP7     COMBINATORIAL ; INPUT  delay line output - 35 ns
PIN   8  W2       COMBINATORIAL ; INPUT
PIN   9  W0       COMBINATORIAL ; INPUT  W0-W2 = code for selection
PIN   10 GND                                     of delay line tap
PIN   11 W1       COMBINATORIAL ; INPUT
PIN   12 IO0                    ; OUTPUT not connected
PIN   13 LINE     COMBINATORIAL ; OUTPUT partial logic, not connected
PIN   14 HC3      COMBINATORIAL ; INPUT  horizontal count from U111
PIN   15 ATC      COMBINATORIAL ; INPUT  vertical count from U111
PIN   16 VLTC     COMBINATORIAL ; INPUT  vertical clock (horiz. lines)
PIN   17 S1       COMBINATORIAL ; INPUT  S0,S1 = code for selection
PIN   18 S0       COMBINATORIAL ; INPUT          of test pattern
PIN   19 XHATCH   COMBINATORIAL ; OUTPUT test pattern output to U108
PIN   20 VCC
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